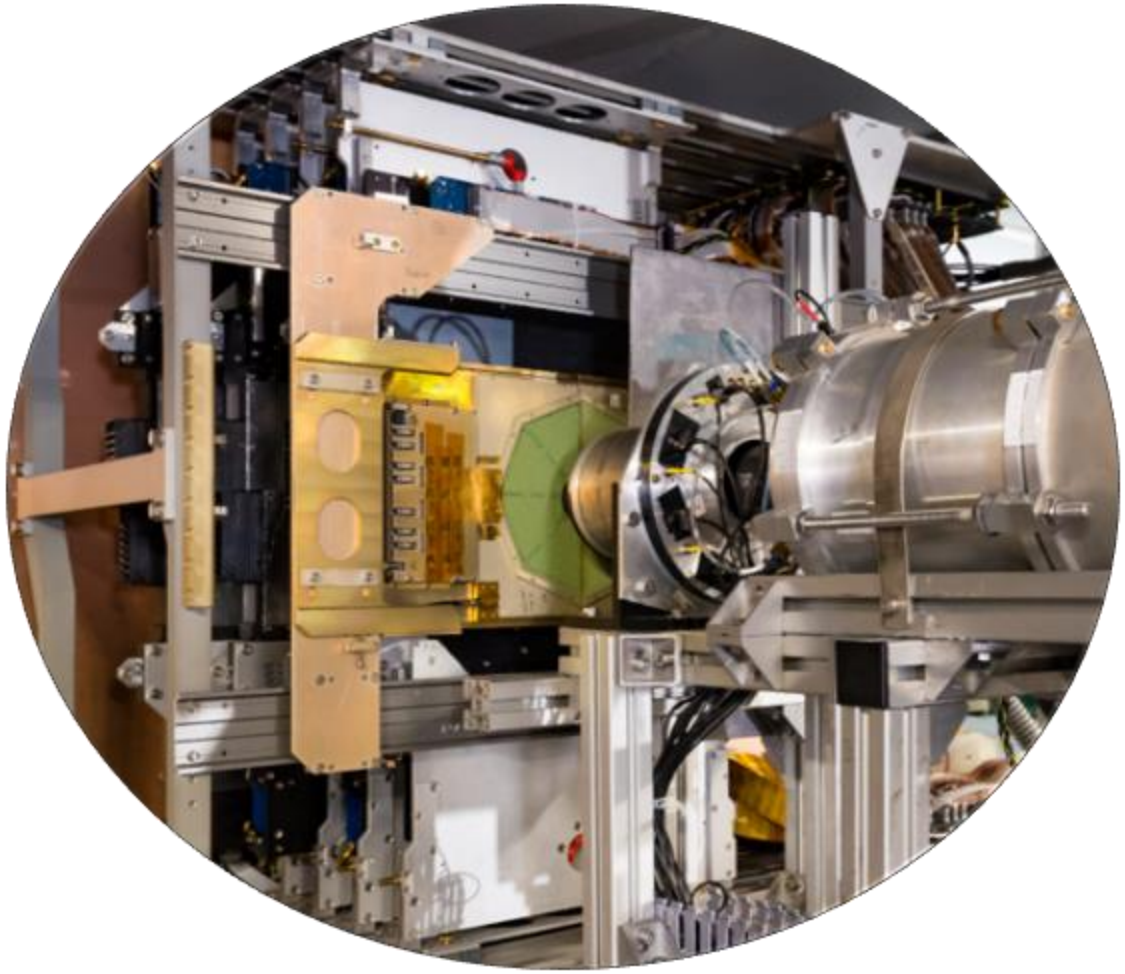
Large-area silicon coordinate module (186×63 mm^2) for the BM@N experiment

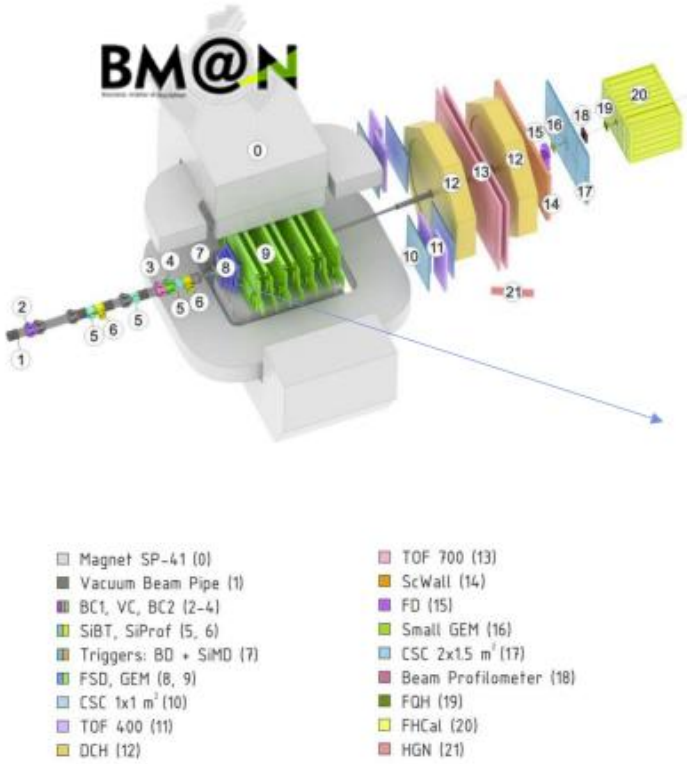
Kopylov Yu .A.
on behalf of the Forward Silicon Detector team

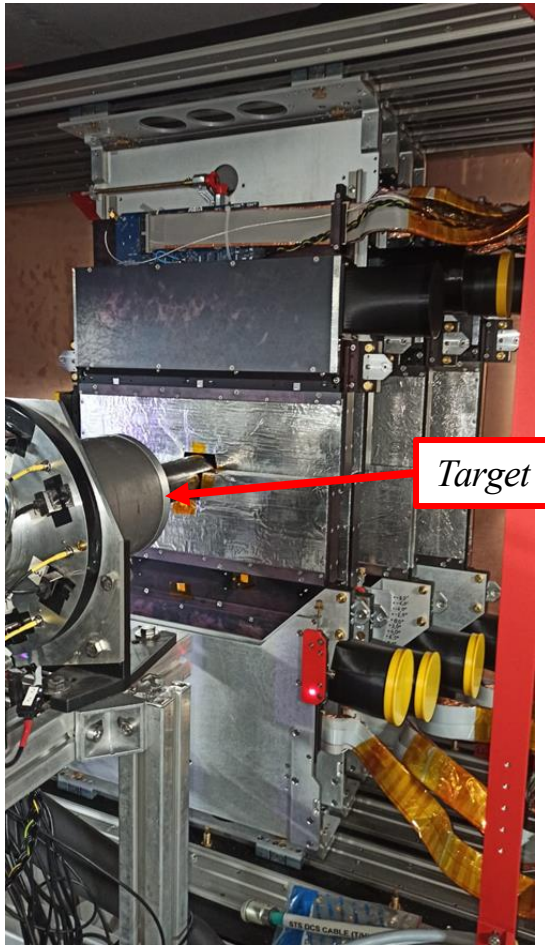


г. Протвино, 05.06.2026

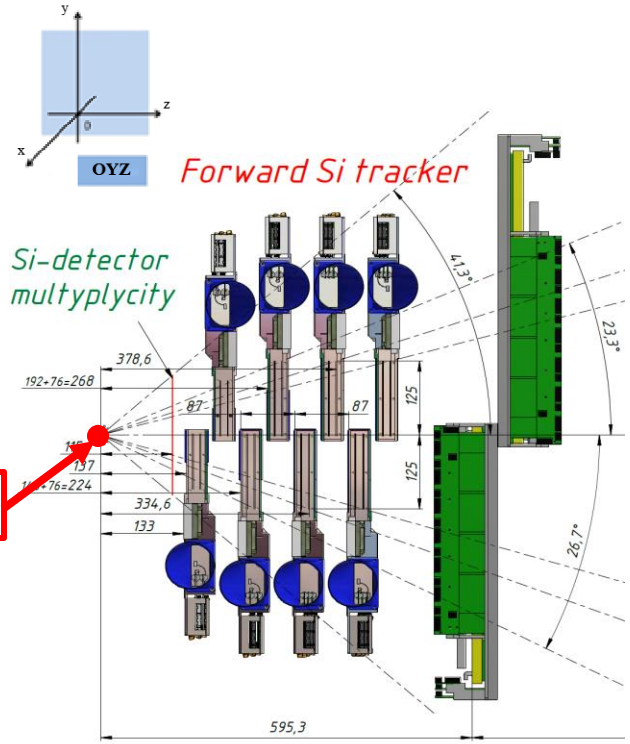
Forward Silicon Detectors Configuration (BM@N 2026 – Xe run)

BM@N (Baryonic Matter at Nuclotron) is the first experiment operational at the **Nuclotron/NICA** ion-accelerating complex, dedicated to studying interactions of relativistic beams of heavy ions with fixed targets in the energy range that allows reaching high densities of baryonic matter.

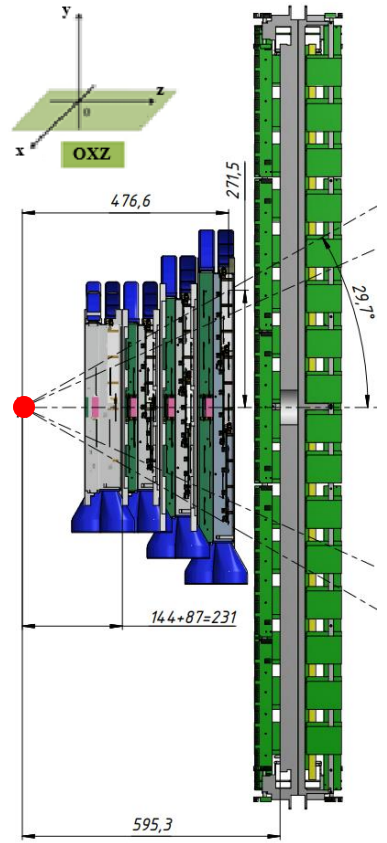




View of the FSD in the magnet SP-41



Location of FSD planes in session 2026 (OYZ side)



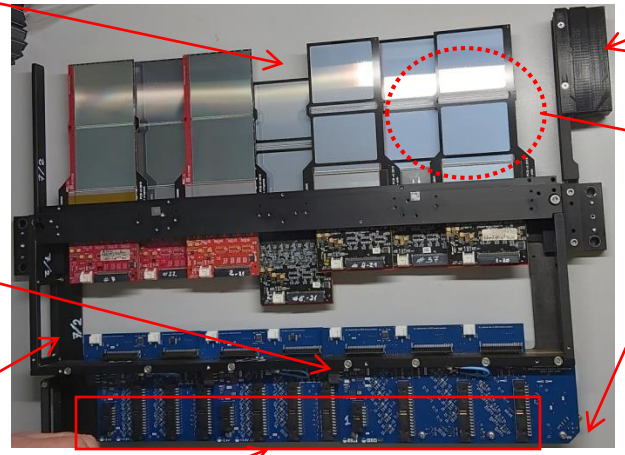
Location of FSD planes in session 2026 (OYZ side)

Planes	#0	#1	#2	#3	Total
Modules	6	10	14	18	48
Channels	7680	12800	17920	23040	61440
Area, cm²	351,54	793,8	1111,32	1428,84	3685,5

Silicon Detector Module

Beam pipe hole

Silicon half-plane with FEE



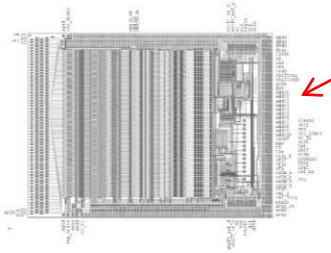
Cooling system output

LV input

Cooling system input

HV input

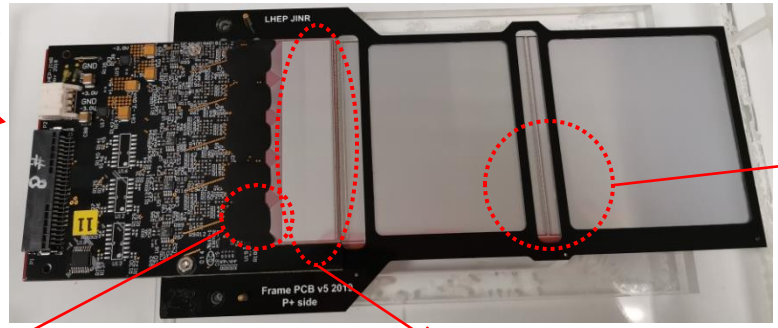
Outputs to DAQ



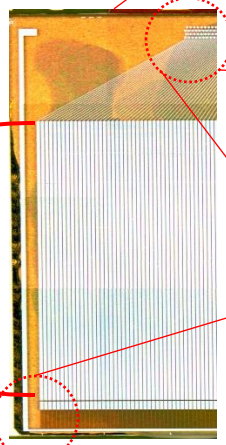
ASIC VATAGP7.2 (5 chips on each side of module)

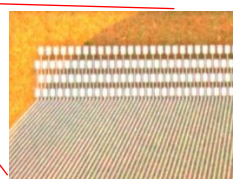
Number of CSA: 128 channels
Dynamic range: ±30 fC
Peaking time (slow/fast shaper): 500 ns/ 50ns
Noise (ENC): 70e +12e/pF (typ.)
Voltage supply: +1,5 V, -2,0 V
Gain from input to output buffer: 16,5 µA/fC
Output Serial analog multiplexer clock speed: 3,9 MHz
Power dissipation per channel: 2,2 mW

Silicon Detector module (p+) side

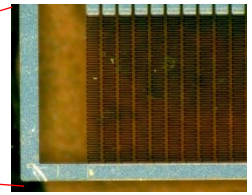


Capacitor





Contact pads

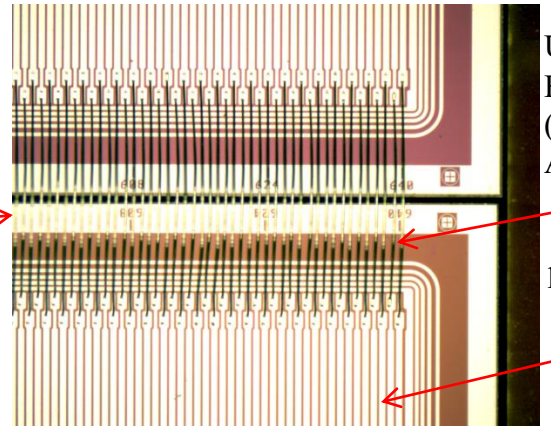


Value of poly-Si resistors

Pitch Adapter (n+) side

Number of channels: 640
Value of poly-Si resistors: ≈ 1 MΩ
Value of integrated capacitors: ≈ 120 pF
Capacitor working voltage: 100 V
Capacitor breakdown voltage: >150 V
Manufactured by ZNTC (Zelenograd)

63000 µm ± 15µm



Ultrasonic Bonding (US- Bonding) Al wire Ø 25 µm

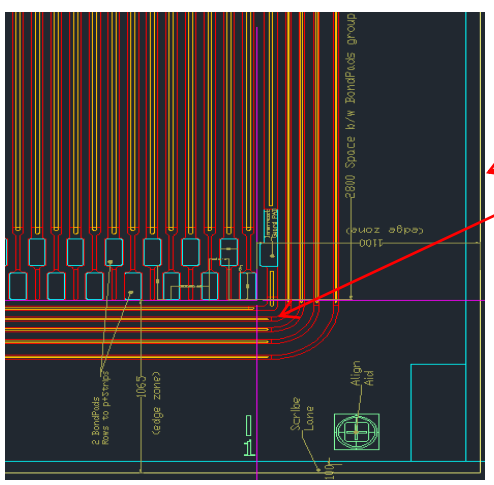
p^+ implantation region

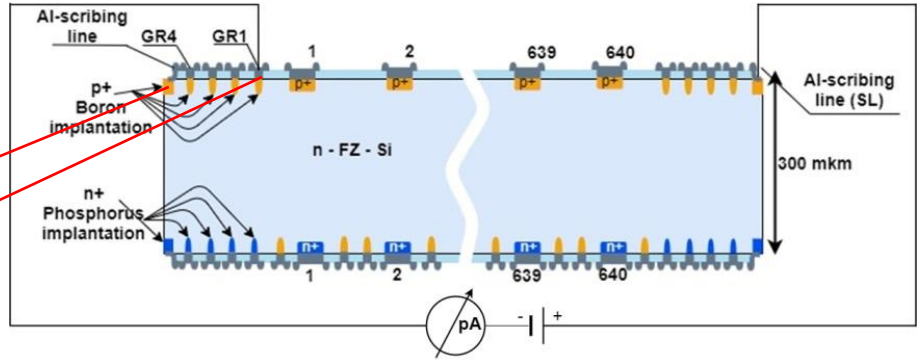
Double sided Silicon detector (p+) side

Size: 63x63x0,3 mm^3 (on 4" – FZ-Si wafers)
Topology: double sided microstrip (DSSD)
(DC coupling)
Pitch p^+ strips: 95 µm;
Pitch n^+ strips 103 µm;
Stereo angle between p^+/n^+ strips: $2,5^0$
Number of strips: 640 (p^+)× 640(n^+)
Development by JINR, RIMST (Zelenograd)
Manufactured by RIMST (Zelenograd)

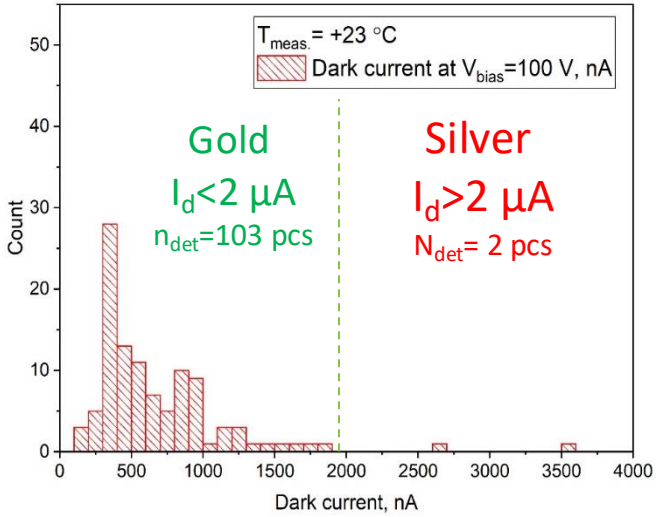
DSSD and Pitch Adapter tests

Basic parameters of DSSD 640×640 for Forward Silicon Tracker

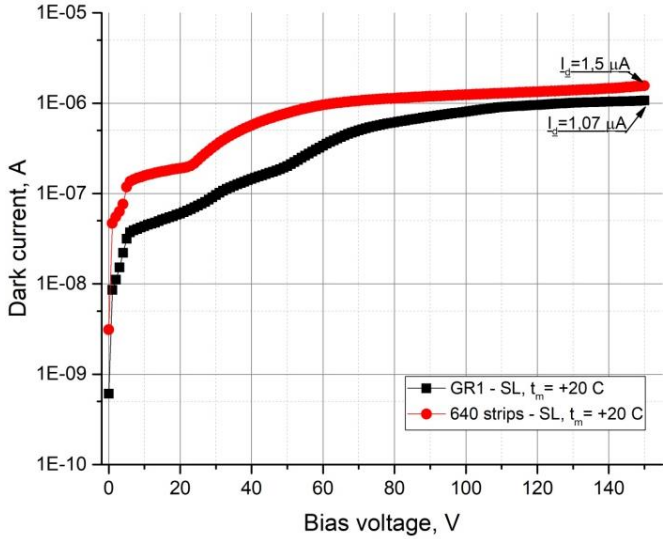




Measurement scheme of summary dark current by using first guard ring and scribing line

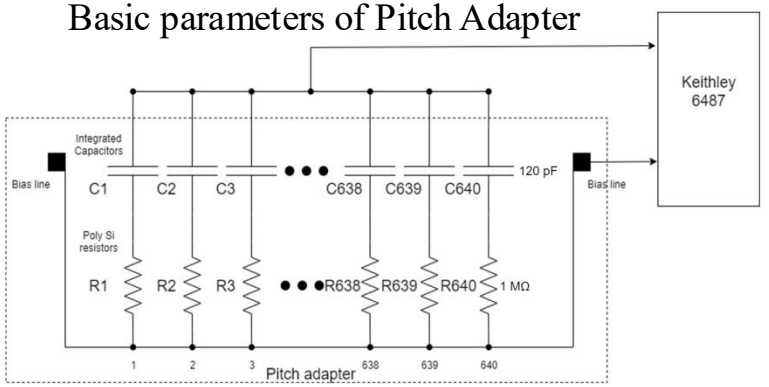


Summary DSSD's Dark Currents at V_{bias} = 100 V and t_m = +23 ºC, RIMST, Zelenograd

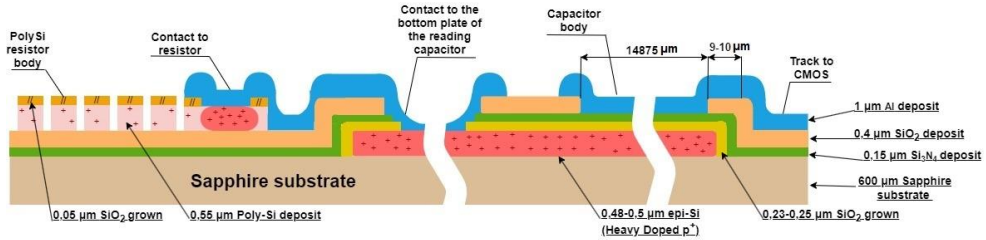


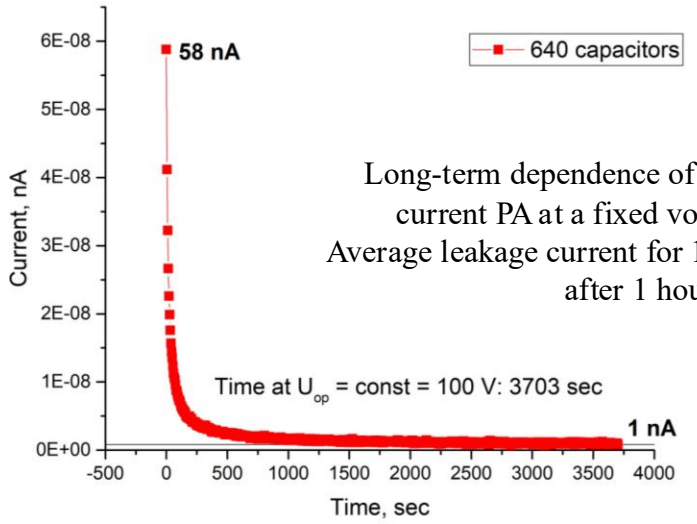
I-Vs for different measurement scheme, t = +20˚

Basic parameters of Pitch Adapter



Measurement scheme of summary leakage current





Long-term dependence of the total leakage current PA at a fixed voltage of 100 V
Average leakage current for 1 capacitor ≈ 1,5 pA after 1 hour

Stages of Assembly and Testing of the Silicon Coordinate Module

Assembly FEE PCBs with PAs

1 Assembly FEE PCBs with ASICs, testing

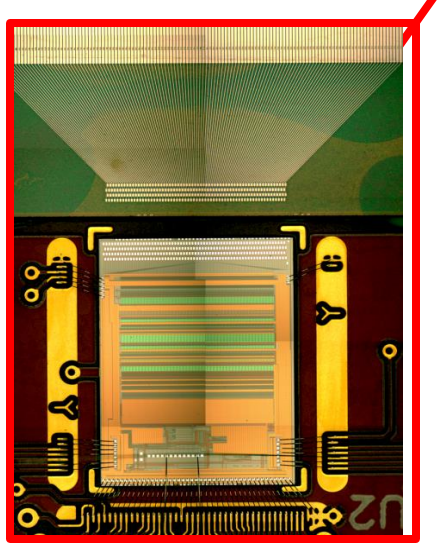
2 Ultrasonic bonding for Pitch Adapter and ASICs

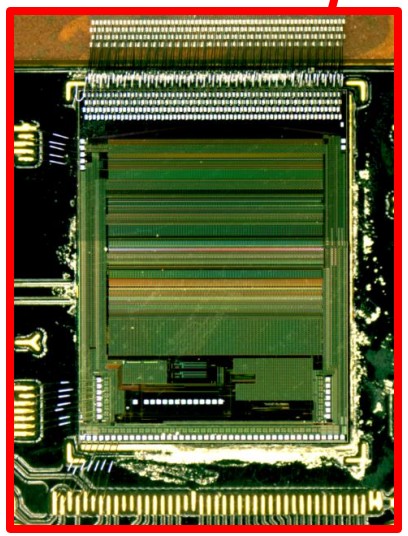
3 Filling ASICs and USB PA with compound

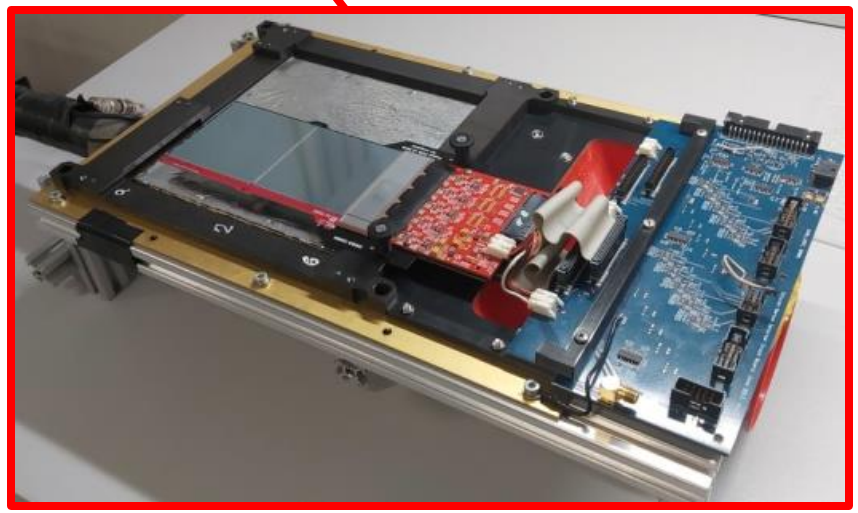
Testing the assembled FEE boards and writing the results to the database

Assembly FEE boards with DSSDs (VBLHEP)

Module testing with β-source and write results to database



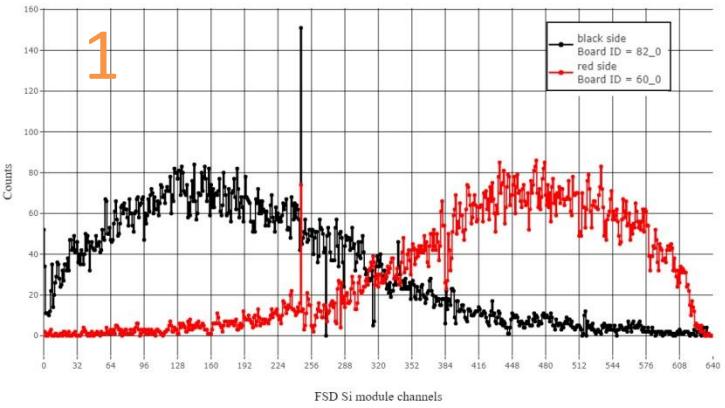


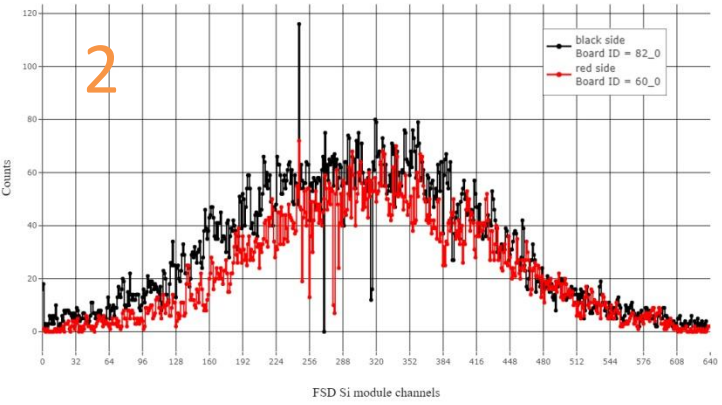


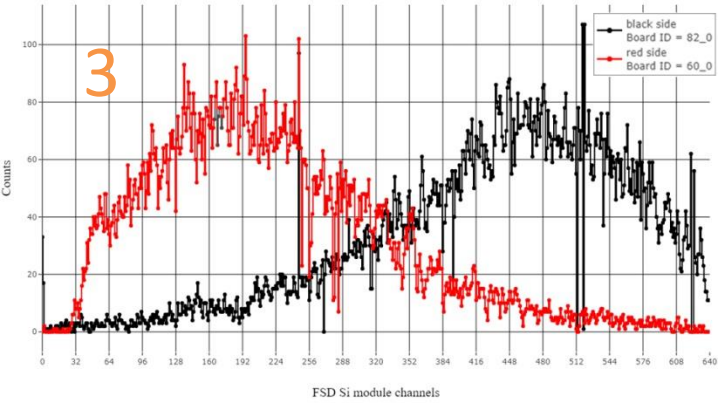
FST Si module test results

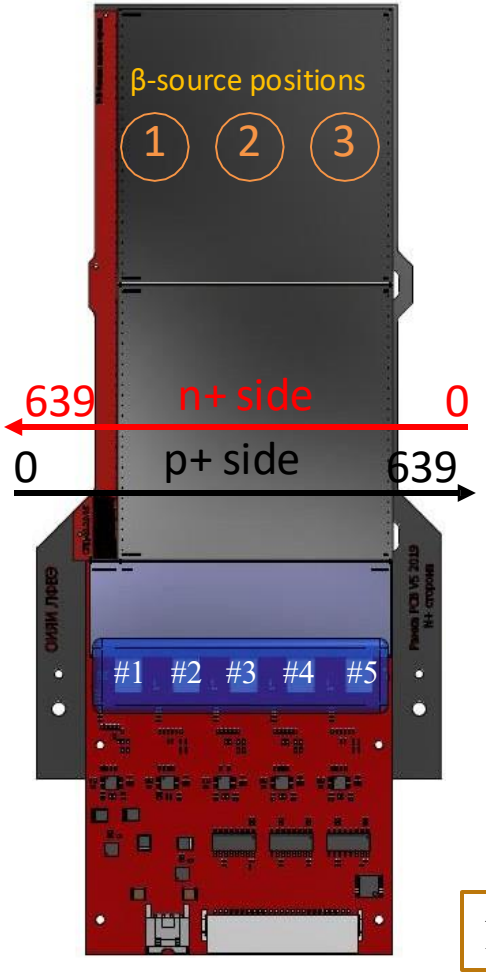
module #42

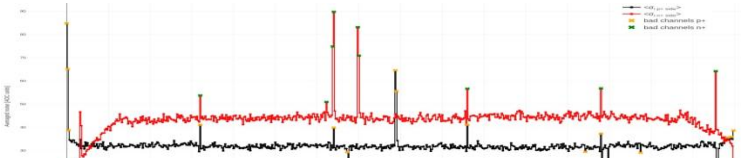
Occupancy distributions in FSD Si module channels after noise suppresion



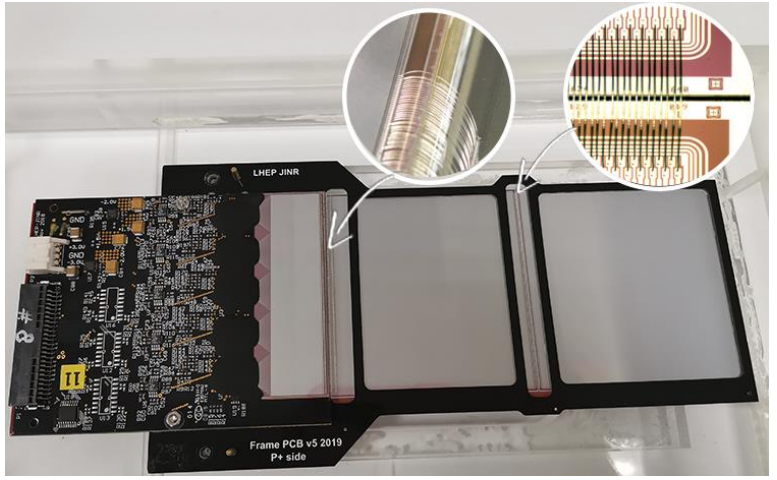






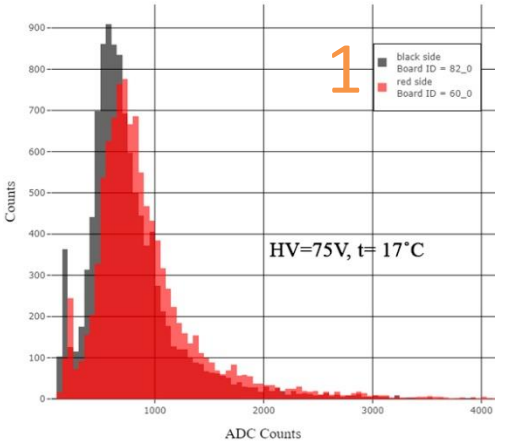


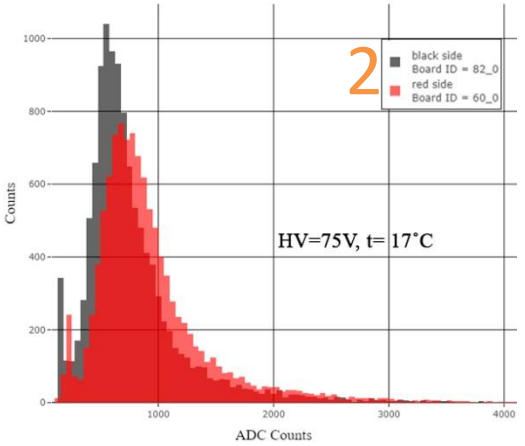
Sigma values of each FSD Si module channels at 75 V

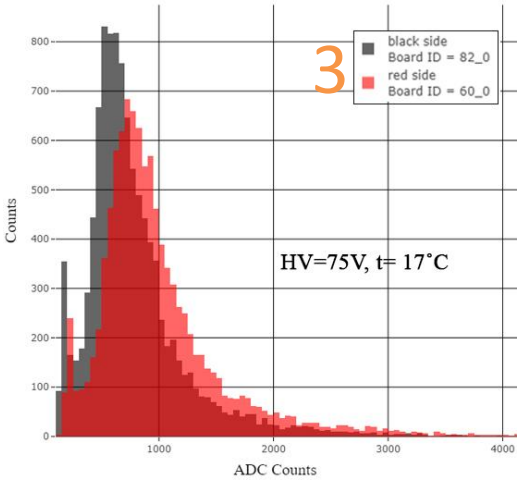


Module view after US- Bonding detectors and PAs, number of US- Bonding – 640, Ø Al wire – 25 µm

1ch. ADC_{p+} = 45 e 1 ch.ADC_{n+}= 42 e



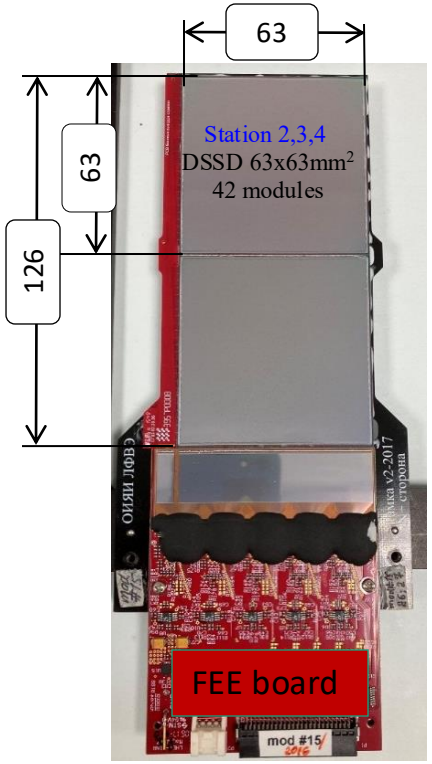




Module ID	Dark current (50V), nA	Mean noise ($^{+}$p), ch.ADC	Mean noise ($^{+}$n), ch.ADC	MPV ($^{+}$p), ch.ADC	MPV ($^{+}$n), ch.ADC	S/N p^{+} side	S/N n^{+} side	Bad channels ratio, %
42_0	3 584,00	36,93	50,76	536,20	578,89	14,09	13,32	0,55

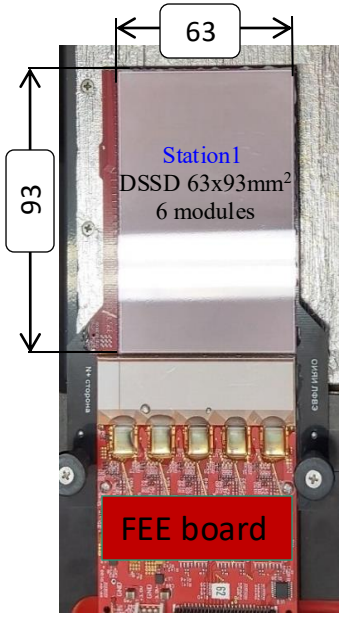
Type of Si-modules for Forward Si detector

The module was developed in 2015



Detectors size: 63x63x0,3 mm³ (on 4" – FZ-Si-n wafers)
Topology: double sided microstrip (DSSD)
(DC coupling)
Pitch p^+ strips: 95 μm;
Pitch n^+ strips 103 μm;
Stereo angle between p^+/n^+ strips: 2.5^0
Number of strips/DSSD: 640 (p^+)×614(n^+)
Number of strips/module: 640 (p^+)×640(n^+)

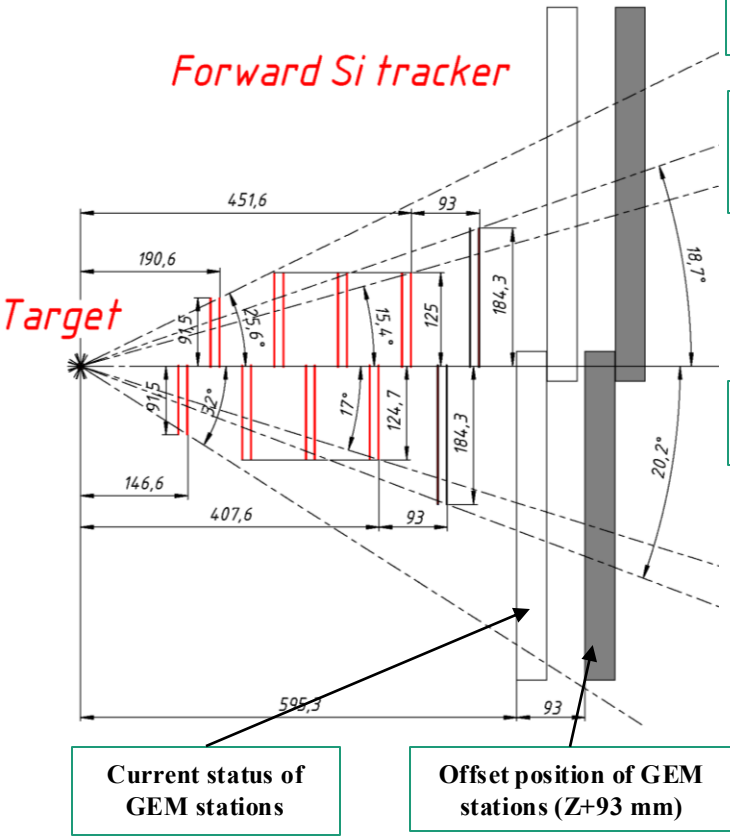
The module was developed in 2020

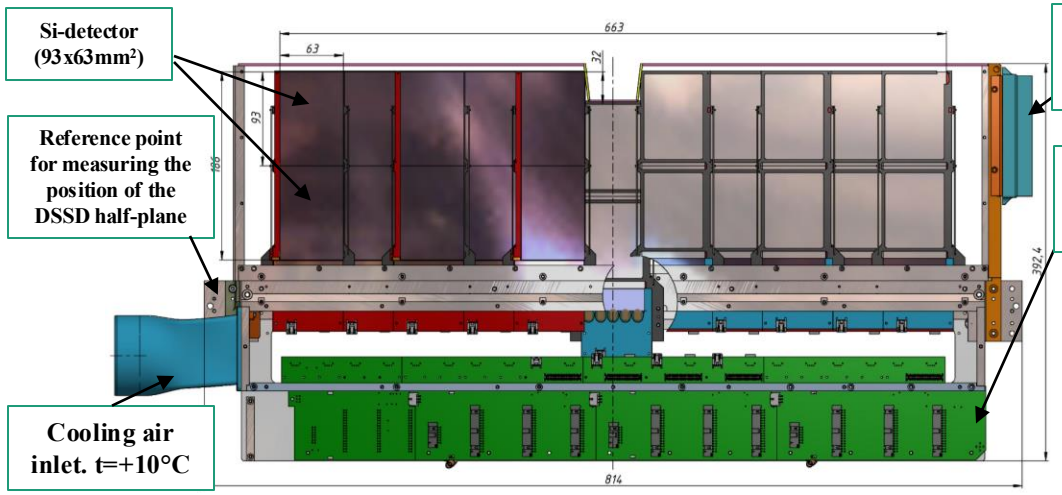


Detectors size: 63×93×0,3 mm³ (on 6" – FZ-Si-n wafers)
Topology: double sided microstrip (DSSD)
(DC coupling)
Pitch p^+ strips: 95 μm;
Pitch n^+ strips 107,1 μm;
Stereo angle between p^+/n^+ strips: 2.5^0
Number of strips/DSSD: 640 (p^+)×603(n^+)
Number of strips/module:640 (p^+)×640(n^+)

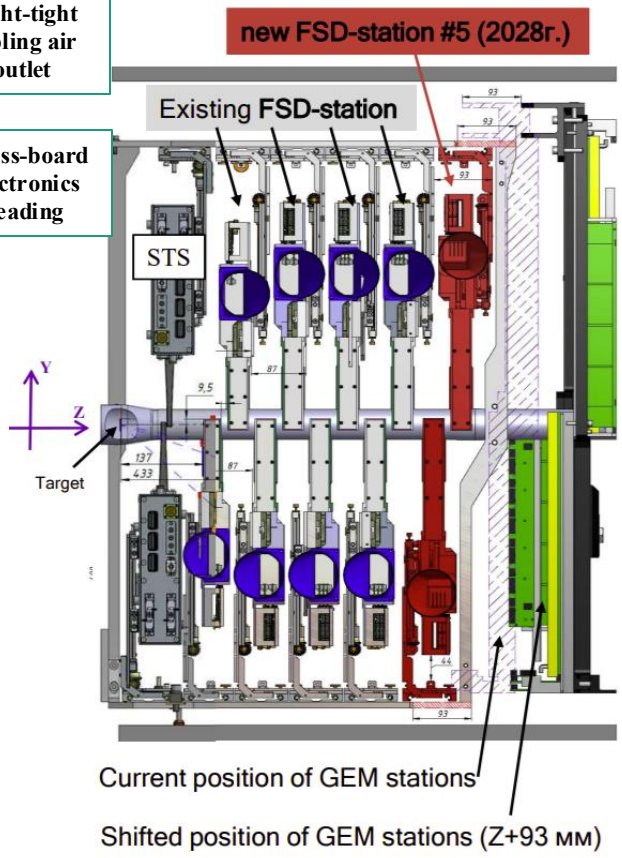
The new 5th plane of the Forward Silicon detector

The development plan for the Forward Silicon Detector includes an additional 5th plane of silicon double-sided strip detectors (DSSD), which is expected to increase the efficiency of primary vertex reconstruction. Therefore, it is necessary to develop and create a prototype of a coordinate module based on DSSD (with a sensitive area of 93 × 63 mm^2) for the upgraded version of the Forward Silicon Detector in the BM@N experiment.



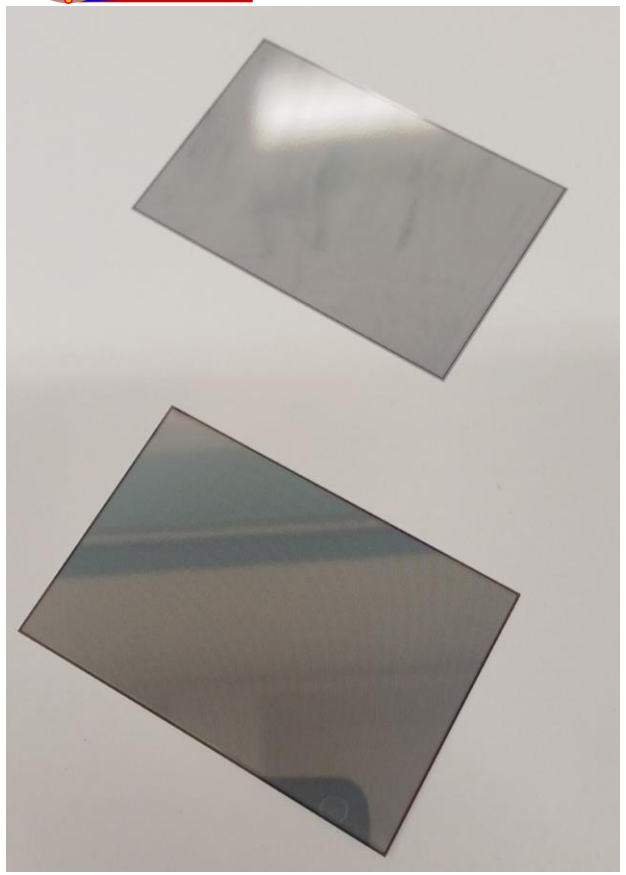


Station	#1	#2	#3	#4	NEW #5!
Module	6	10	14	18	22
Type DSSD, mm^2	63 × 93	63 × 63	63 × 63	63 × 63	63 × 93
Quantity of used DSSD	1	2	2	2	2
Sensitive area of the module, mm^2	5859	7938	7938	7938	11718
Sensitive area of the station, mm^2	351,54	793,8	1111,32	1428,84	2577,96

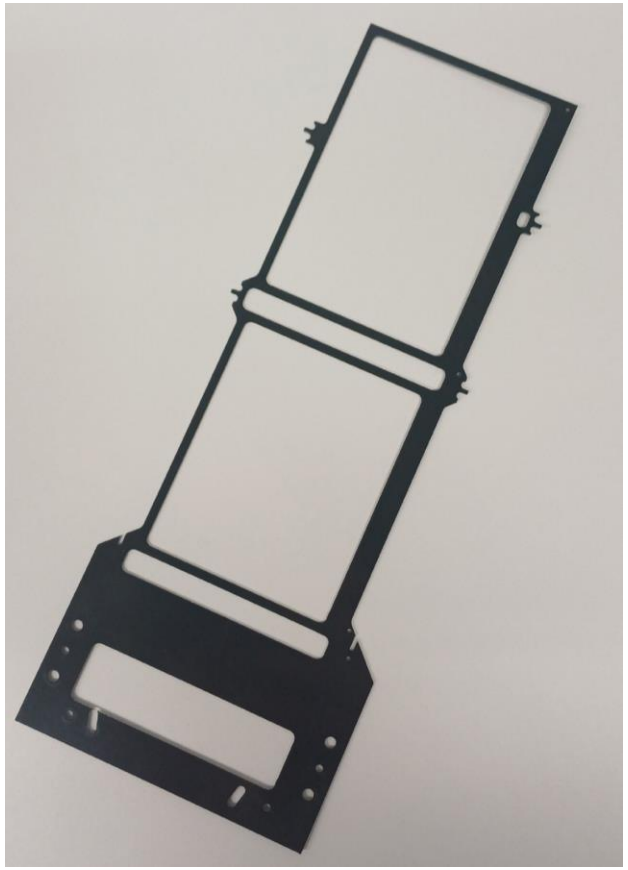


The sensitive area of the new 5th station will be 1.8 times larger than the *4th station*, which currently has the largest sensitive area!!!

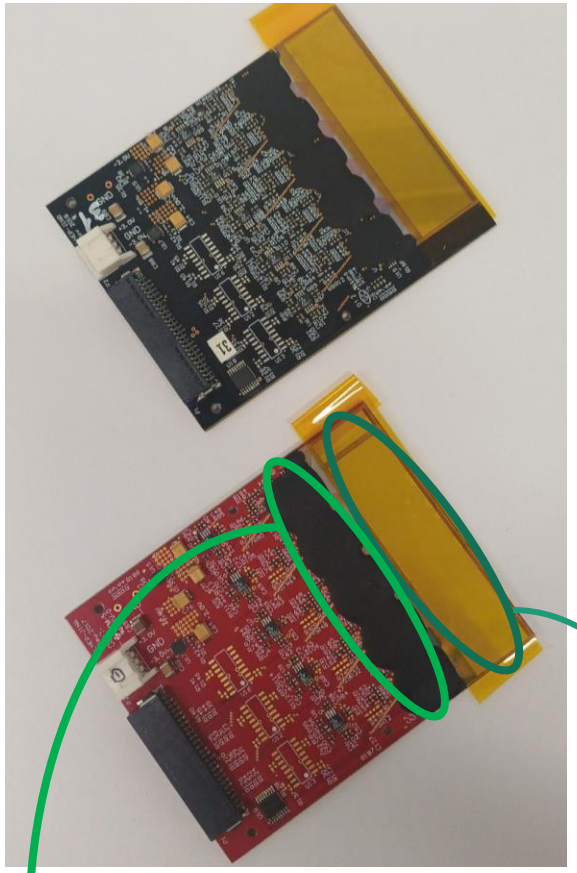
Components for building a new module



Detectors size: 63×93×0,3 mm^3 (on 6” – FZ-Si-n wafers)
Topology: double sided microstrip (DSSD)
(DC coupling)
Pitch p^+ strips: 95 μm;
Pitch n^+ strips 107,1 μm;
Stereo angle between p^+/n^+ strips: 2.5^0
Number of strips/DSSD: 640 (p^+)×603(n^+)
Number of strips/module:640 (p^+)×640(n^+)
Development by JINR, RIMST (Zelenograd)
Manufactured by RIMST (Zelenograd)



Position frame



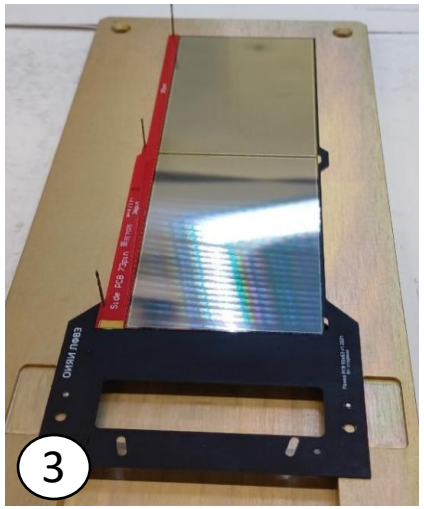
Front-End Electronics (FFE)

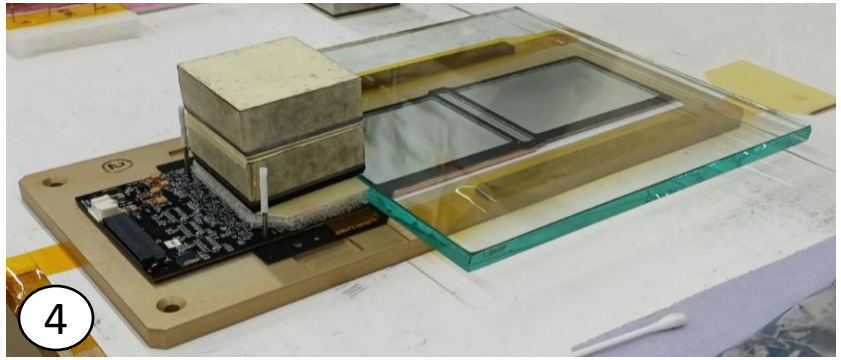
ASIC VATAGP7.2 (5 chips on each side of module)
Number of CSA: 128 channels
Dynamic range: ±30 fC
Peaking time (slow/fast shaper): 500 ns/ 50ns
Noise (ENC): 70e +12e/pF (typ.)
Voltage supply: +1,5 V, -2,0 V
Gain from input to output buffer: 16,5 μA/fC
Output Serial analog multiplexer clock speed: 3,9 MHz
Power dissipation per channel: 2,2 mW

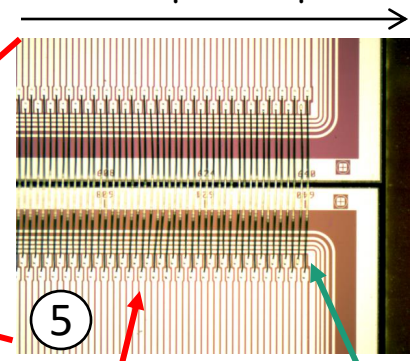
Pitch Adapter side
Number of channels: 640
Value of poly-Si resistors: ≈ 1 MΩ
Value of integrated capacitors: ≈ 120 pF
Capacitor working voltage: 100 V
Capacitor breakdown voltage: >150 V
Manufactured by ZNTC (Zelenograd)

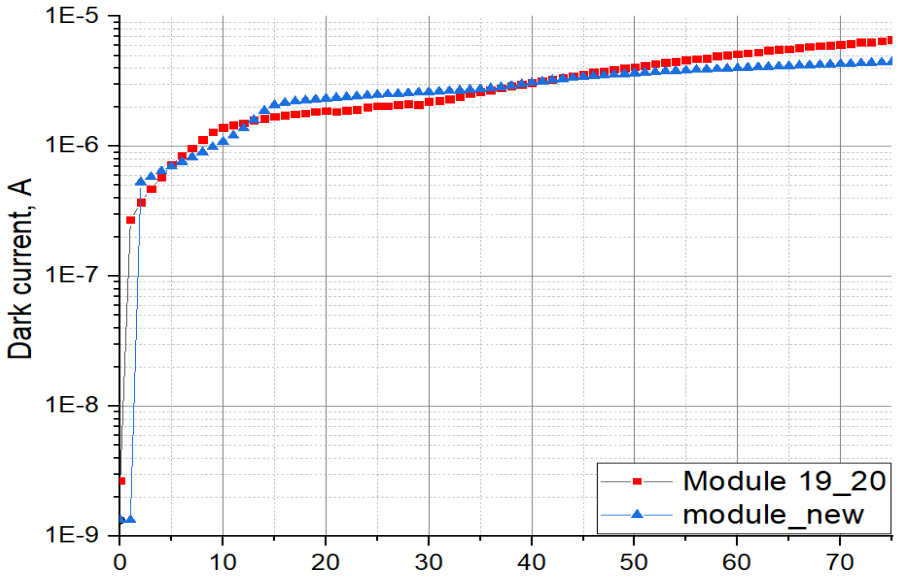
The process of assembling a new coordinate module (186 × 63) mm²

1. For each side of the module, the selection and input control of the FEE boards were carried out;
2. Using mechanical equipment the process of combining and fixing two DSSD (186 × 63) mm² with a position frame was carried out;
3. The process of installing a PCB board (on a position board) designed to collect the signal from the long distance n+ strips of the detector was performed;
4. The selected FFE boards were mounted on the position board;
5. Ultrasonic welding was used to ensure reliable contact between the DSSD strips and the Pitch - Adapter pads (on the FFE);
6. The module is fully assembled and ready for testing.





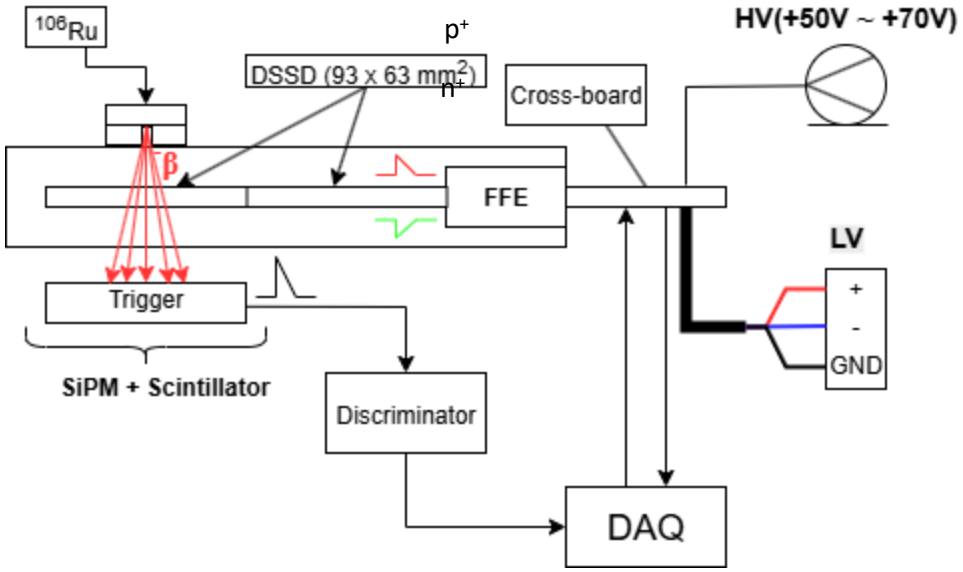


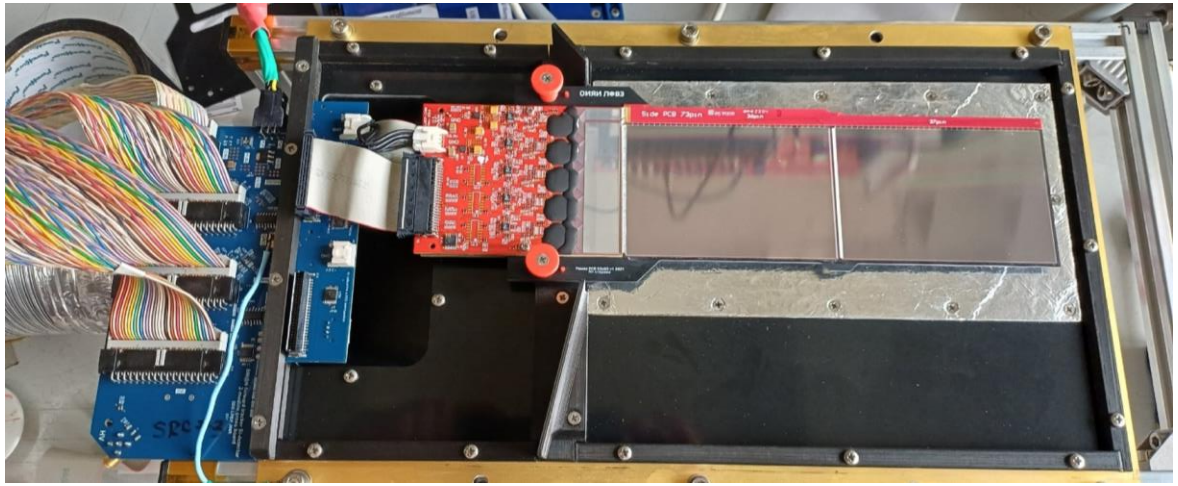


Module	Type DSSD, mm²	Sensitive area of the module, mm²	Temperature, °C
19_20	63 × 63	126 × 63	23.89
NEW	93 × 63	186 × 63	23.74

The test bench of the new coordinate module

Basic measuring circuit

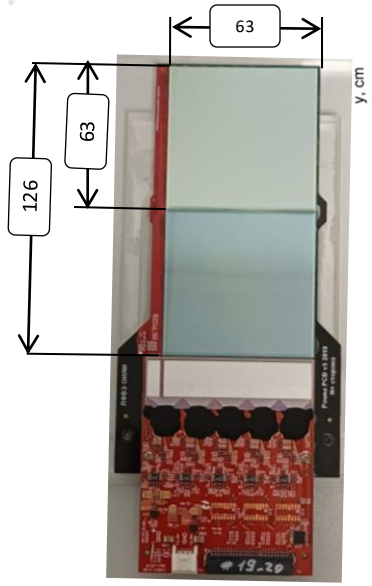


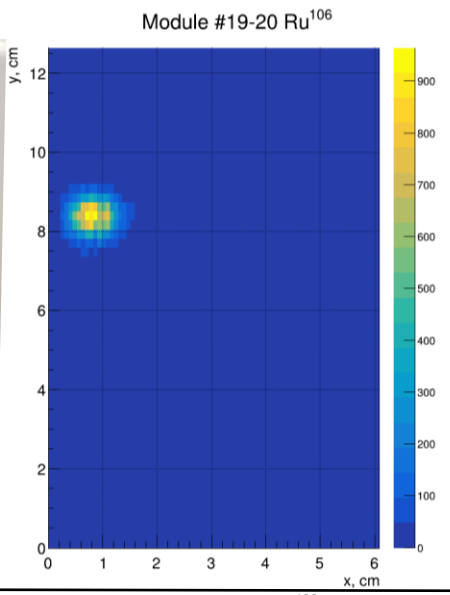


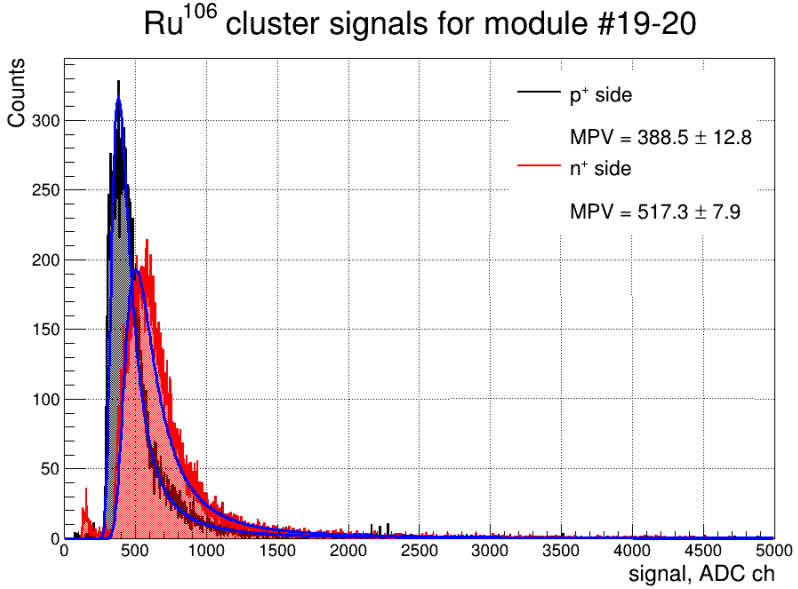
Location of the NEW Module (186 × 63 mm^2)
inside the test box (without the cover plate)

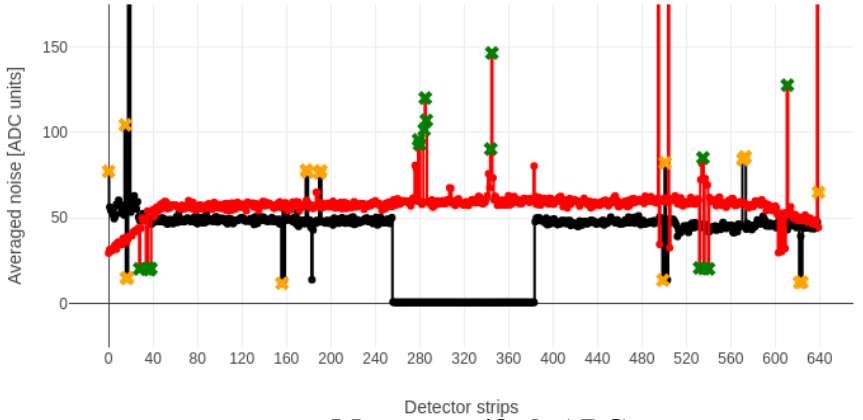
Comparison of results with the previous version of coordinate modules

Standard module







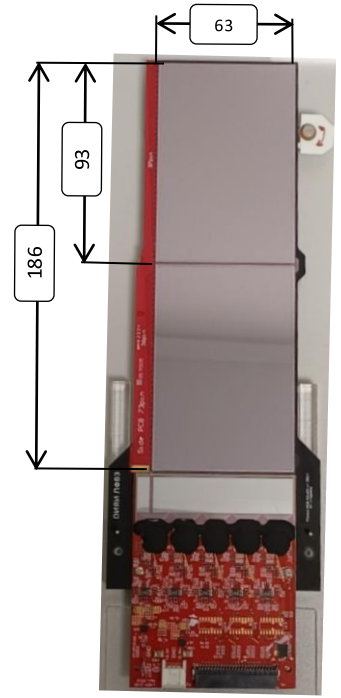


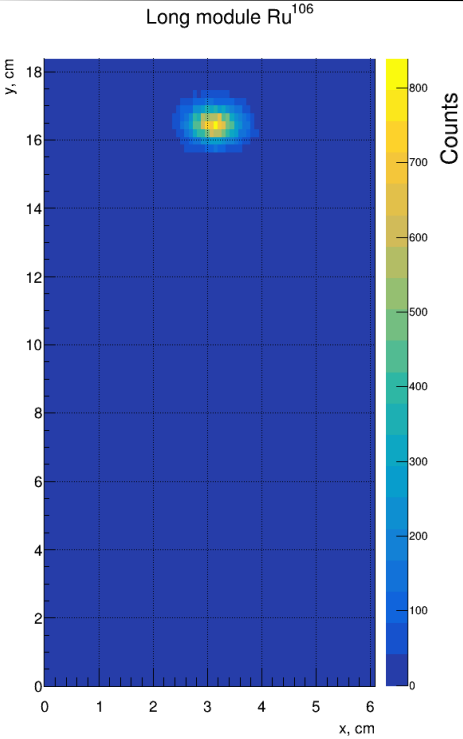
Mean σ_{p+}=48 ch.ADC

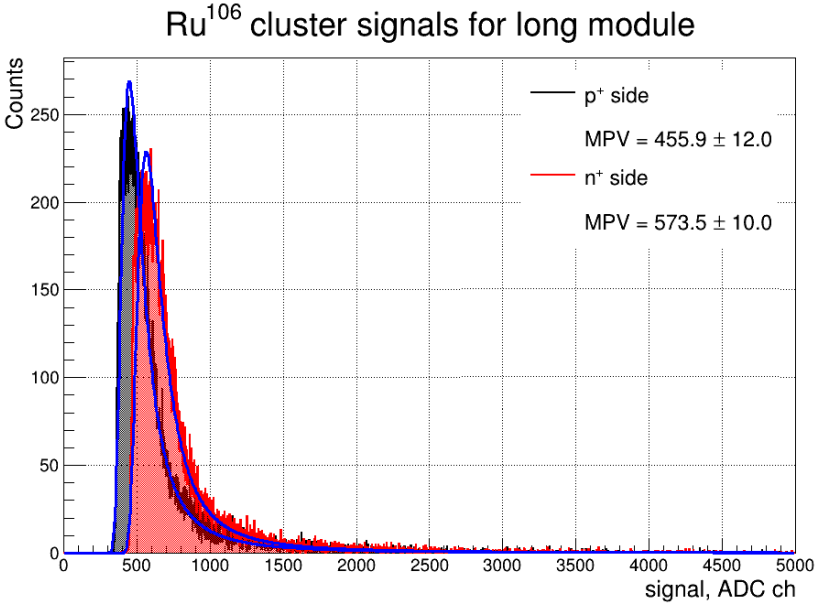
Mean σ_{n+}=59 ch.ADC

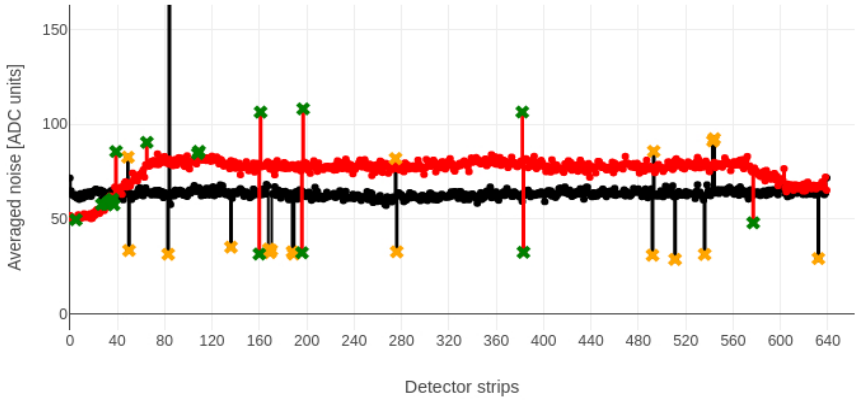
S/N = 8.45

New module!









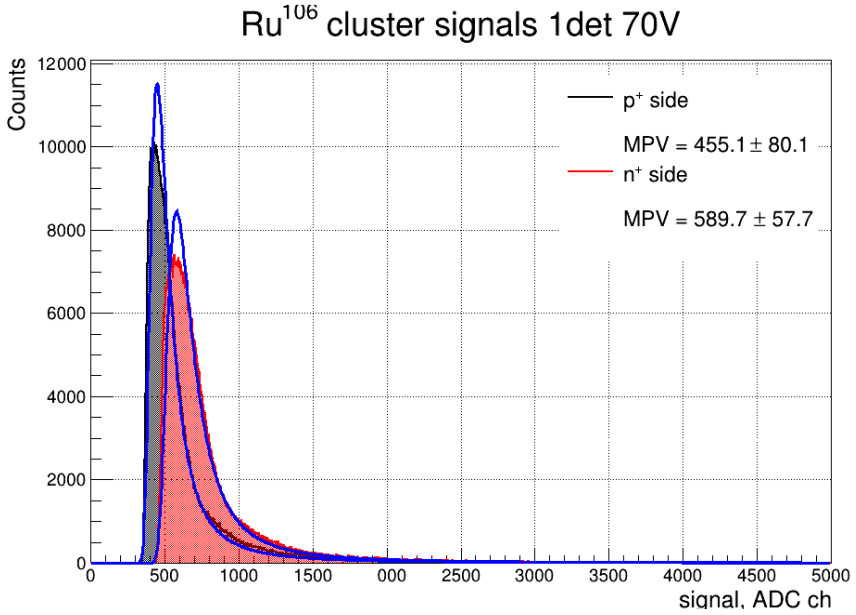
Mean σ_{p+}=60 ch.ADC

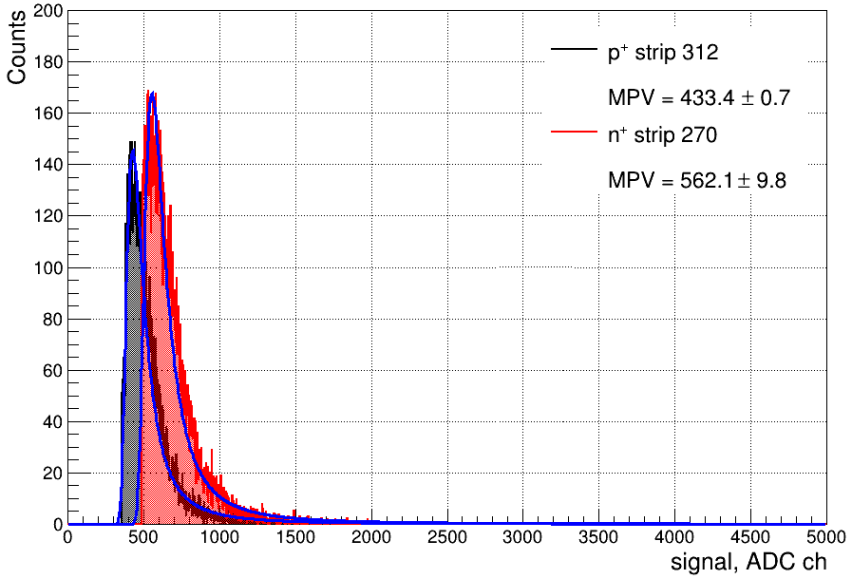
Mean σ_{n+}=76 ch.ADC

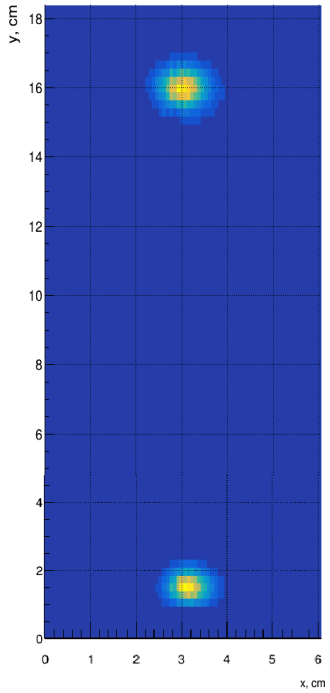
S/N =7.6

Test (β-source, ^{106}Ru) results of the coordinate module with DSSD (186 × 63)mm^2

det. # 1

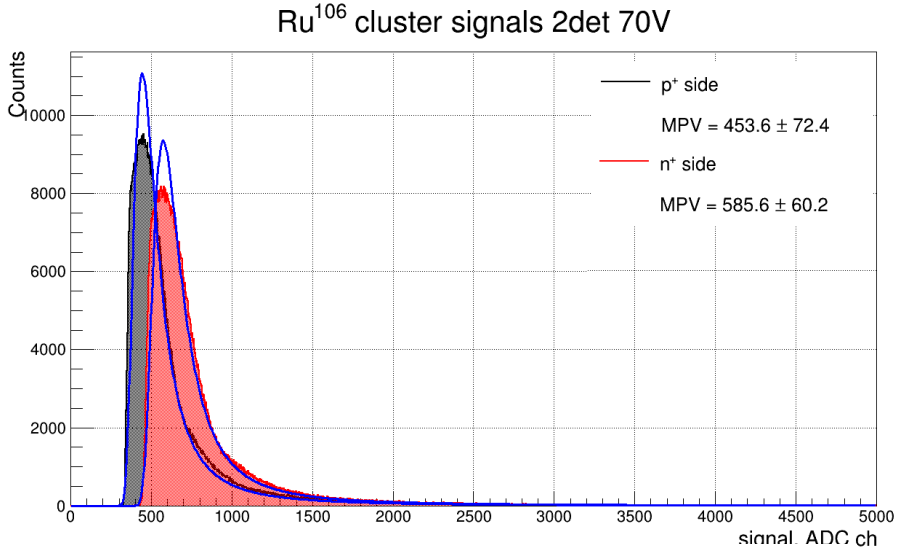


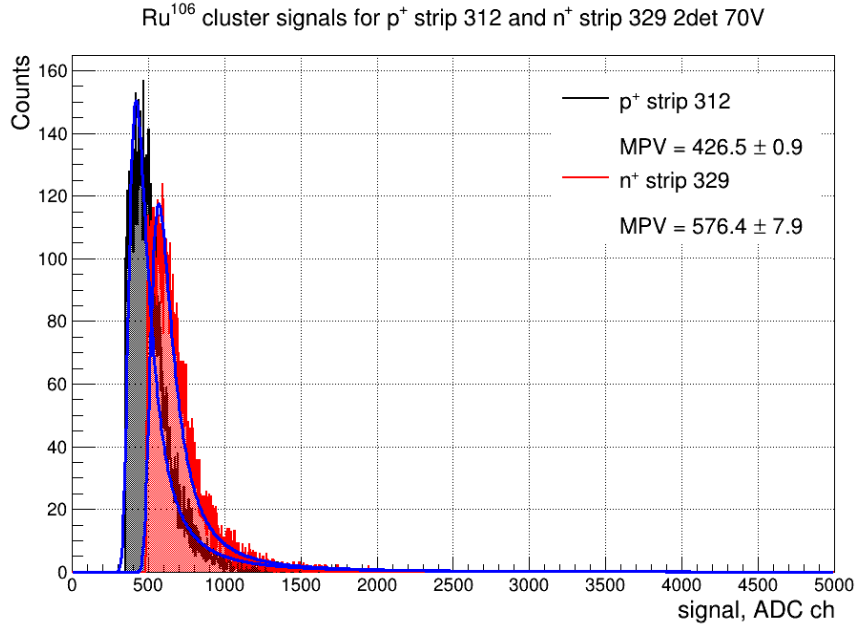




S/N = 7.6

det. # 2





Conclusions

The assembly and first tests of a prototype of a new silicon module with a sensitive area of 186 × 63 mm^2 have been successfully completed. A workable design has been created that confirms the basic functionality.
Fine-tuning and detailed study of the module's performance characteristics are currently underway.

Forward Silicon Detector team

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Thank you for your attention!